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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/527,497 | 03/16/2000 | Sunil C. Shah | 001340,zp006q | 2379 |

7590 08/28/2003

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| EXAMINER | |
|---|---|
| THOMSON, WILLIAM D | |
| ART UNIT | PAPER NUMBER |
| 2123 | |

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/527,497 | SHAH, SUNIL C. |
| | Examiner | Art Unit |
| | William D. Thomson | 2123 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 March 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. Claims 1-15 have been submitted for examination.

2. Claims 1-15 have been examined and rejected.

### Drawings

3. Applicant filed informal drawings for the instant specification on March 16, 2000. These drawings are acceptable for examination purposes. The drawings have not been reviewed by the draftsman since a number of issues are present in the figures.

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See M.P.E.P § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

## PRIOR ART REJECTIONS

### *Claim Rejections - 35 U.S.C. § 102*

4. Claims have been afforded their broadest reasonable interpretation. Applicant's language directed to diagram and ordering of blocks has been interpreted as the standard features provided in windows based GUI SPICE simulators that allow the user

to reorder the circuits during simulations, add circuit layouts and simulate the changes in a graphical environment. The retro events and backtracking events to reorder and improve the simulation blocks of the applied art are equivalent to the recitations of ordering the blocks in the block diagram structure.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kazmierski et al. (217).

Taking claim 1, for example Kazmierski et al. (217) teaches:

A method for simulation modeling where the simulation model includes individual blocks in a block diagram structure wherein each of the individual blocks include equation sets of a physical model, comprising the steps of: (see Abstract, Figures 1-10, Summary of the Invention, col. 4, lines 34 et seq.)

configuring said blocks in a block diagram structure; (col. 4, lines 34 et seq., figures 1-10)

utilizing commercial simulation software to solve said equation sets of

said blocks; (col. 6, lines 33-40, SPICE)

ordering said blocks in said block diagram structure to allow for waveform relaxation of sets of variables of said blocks; and (col. 5, lines 5 et seq, )

performing waveform relaxation of said sets of variables of said blocks. (col. 4, lines 34 et seq.)

As to claim 2, the method of claim 1, wherein said step of ordering said blocks in said block diagram structure includes decomposing said block diagram into subsystems is taught within Kazmierski et al. (217) at col. 5, lines 5 et seq.

As to claim 3, the method of claim 1, wherein said step of ordering said blocks in said block diagram structure includes identifying said sets of variables of said blocks is taught within Kazmierski et al. (217) at col. 5, lines 5 et seq.

As to claim 4, the method of claim 1, wherein said step of ordering said blocks in said block diagram structure includes adding a low fidelity model of one of said blocks is taught within Kazmierski et al. (217) at col. 5, lines 5 et seq.

As to claim 5, the method of claim 4, wherein said sub-step of adding said low fidelity model of one of said blocks includes deriving an error signal from an output of said one of said blocks and an output of said low fidelity model is taught within Kazmierski et al. (217) at col. 5, lines 5 et seq.

As to claim 6, the method of claim 5, wherein said step of ordering said blocks in said block diagram structure includes accelerating convergence of said simulation model by processing said error signal is taught within Kazmierski et al. (217) at col. 6, lines 58 et seq.

As to claim 7, the method of claim 1, wherein said step of performing waveform relaxation includes deriving a sparse interconnect matrix is taught within Kazmierski et al. (217) at col. 6, lines 58 et seq.

As to claim 8, the method of claim 7, wherein said step of performing waveform relaxation includes weakly-coupling said equation sets is taught within Kazmierski et al. (217) at col. 5, lines 65 et seq.

As to claim 9, the method of claim 8, wherein said step of utilizing said commercial simulation software includes running said commercial simulation software on a plurality of data processors is taught within Kazmierski et al. (217) at col. 6, lines 34 et seq.

As to claim 10, the method of claim 9, wherein said step of running said commercial software on said plurality of data processors includes waiting until each of said commercial simulation software has completed calculations before transmitting interprocessor communications data (IPC and API) is taught within Kazmierski et al. (217) at col. 7, lines 8 et seq., and col. 9, lines 4 et seq.

As to claim 11, the method of claim 1, wherein said equation sets change in subsequent iterations of said simulation model is taught within Kazmierski et al. (217) at col. 6, lines 58 et seq.

As to claim 12, the method of claim 11, wherein said equation sets increase in fidelity in subsequent iterations of said simulation model is taught within Kazmierski et al. (217) at col. 6, lines 58 et seq.

As to claim 13, the method of claim 1, wherein said step of performing waveform relaxation utilizes Gauss-Jacobi methods is taught within Kazmierski et al. (217) at col. 8, lines 37-44.

As to claim 14, the method of claim 1, wherein said step of performing waveform relaxation utilizes Gauss-Seidel methods is taught within Kazmierski et al. (217) at col. 8, lines 37-44.

Claims 15 is rejected based on the same reasoning as claim 1, *supra*. Kazmierski et al. (217).

**Conclusion**

6. The prior art made of record, see PTO 892, and not relied upon is considered pertinent to Applicant's disclosure, careful consideration should be given prior to Applicant's response to this Office Action.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this action. Failure to respond within the period for response will result in ABANDONMENT of the application (see 35 U.S.C. 133, M.P.E.P. 710.02, 710.02(b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Thomson whose telephone number is (703) 305-0022. The examiner can be usually reached between 9:30 a.m. - 4:00 p.m.

Monday thru Friday. Voice mail is checked throughout the day. Please leave a detailed message including the serial number.

Facsimile numbers are as follows:

Official: 703-746-7239

Draft: 703-746-7240

After Final: 703-746-7238

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Kevin Teska, can be reached on 704-305-9704.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 703-305-3900.

William D. Thomson

Patent Examiner

A.U. 2123

August 21, 2003